a first cladding layer formed on said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer.

17. A semiconductor device comprising:

a substrate;

crystals formed on said substrate and containing at least A1 and N, said crystals being disposed so as to expose portions of said substrate;

a thermal distortion reducing layer made of $A1_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said crystals and having a different chemical formula from that of said crystals;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer.

24. A semiconductor device comprising:

a substrate;

a buffer layer formed on said substrate and comprising a first layer made of $A1_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) and a second layer made of $A1_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said first layer and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said buffer layer comprises means for controlling polarity of a growth surface, said growth surface comprising at least a portion of a surface of said substrate.

31. A semiconductor device comprising:

a substrate;

a buffer layer formed on said substrate and made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \le s \le 1$, $0 \le t \le 1$, $s+t \le 1$);

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \le u \le 1$, $0 \le v \le 1$, $u+v \le 1$) formed on said buffer layer and having a different chemical formula from that of said buffer layer;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said buffer layer comprises means for controlling polarity of a growth surface of said thermal distortion reducing layer, said growth surface comprising at least a portion of a surface of said substrate.

54. A semiconductor device comprising:

a substrate;

a buffer layer comprising a first layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \le s \le 1$, $0 \le t \le 1$, $s+t \le 1$) formed on said substrate;

a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \le u \le 1$, $0 \le v \le 1$, $u+v \le 1$) formed on said first layer and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said first layer comprises pinholes.

64. A semiconductor device comprising:

a substrate;

a buffer layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) formed on said substrate;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed on said buffer layer and having a different chemical formula from that of said buffer layer;

a first cladding layer formed over said thermal distortion reducing layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer,

wherein said buffer layer comprises crystals formed on said substrate, said crystals having intervals therebetween so as to expose said substrate.

74. A semiconductor device comprising:

a substrate;

a buffer layer comprising a first layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) formed on said substrate and a second layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1$, $0 \leq v \leq 1$, $u+v \leq 1$) formed to contact said first layer and said substrate and having a different chemical formula from that of said first layer;

a first cladding layer formed over said second layer;

an active layer formed over said first cladding layer; and

a second cladding layer formed over said active layer.

Please add the following new claims:

76. A semiconductor device comprising:

a buffer semiconductor layer made of $Al_{1-s-t}Ga_sIn_tN$ ($0 \leq s \leq 1$, $0 \leq t \leq 1$, $s+t \leq 1$) and having a number of pinholes formed therein;

a thermal distortion reducing layer made of $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1, 0 \leq v \leq 1, u+v \leq 1$) formed on said buffer semiconductor layer and having a different chemical formula from that of said buffer semiconductor layer;

a first cladding layer formed on said thermal distortion reducing layer;

an active layer formed on said first cladding layer; and

a second cladding layer formed on said active layer.

77. The semiconductor device according to claim 76, wherein, in said $Al_{1-u-v}Ga_uIn_vN$ ($0 \leq u \leq 1, 0 \leq v \leq 1, u+v \leq 1$) for said thermal distortion reducing layer, v is set to be not less than 0.1 and not more than 0.9.

78. A semiconductor device according to claim 76, wherein a film thickness of said thermal distortion reducing layer is greater than that of said semiconductor layer.

79. The semiconductor device according to claim 76, further comprising a cap layer on said thermal distortion reducing layer to prevent evaporation of In included in said thermal distortion reducing layer.

80. The semiconductor device according to claim 79, wherein said cap layer is made of $Al_{1-x}Ga_xN$ ($0 \leq x \leq 1$) and is formed at 500° C. to 800° C.

81. The semiconductor device according to claim 76, wherein said first cladding layer is made of $Al_{1-x-y}Ga_xIn_yN$ ($0 \leq x \leq 1, 0 \leq y \leq 1, x+y \leq 1$).

82. The semiconductor device according to claim 76, wherein said thermal distortion reducing layer has a thickness of 50 nm to 1000 nm.

83. A semiconductor device according to claim 76, further comprising a single crystal substrate on which said semiconductor layer is formed.

84. The semiconductor device according to claim 76, comprising:

a substrate;

said buffer semiconductor layer being formed on said substrate; and

said pinholes comprising exposed portions of said substrate through said buffer semiconductor layer.

85. The semiconductor device according to claim 76, wherein:

said buffer semiconductor layer comprises crystals formed spaced apart; and

said pinholes comprise spaces between said crystals.

86. The semiconductor device according to claim 76, wherein:

said buffer semiconductor layer comprises crystals loosely formed; and

said pinholes comprise spaces between said crystals.

87. The semiconductor device according to claim 76, wherein:

said buffer semiconductor layer consists of an AlGaN material.

88. The semiconductor device according to claim 76, wherein:

said buffer semiconductor layer consists of an AlN material.

89. The semiconductor device according to claim 76, wherein:

said thermal distortion reducing layer consists of a GaN material.

90. The semiconductor device of claim 76, comprising:

a substrate, said buffer semiconductor layer being formed on said substrate.

91. The semiconductor device according to claim 11, wherein:

said buffer semiconductor layer consists essentially of an AlGaN material.

92. The semiconductor device according to claim 11, wherein:

said buffer semiconductor layer consists essentially of an AlN material.

93. The semiconductor device according to claim 11, wherein:

said thermal distortion reducing layer consists essentially of a GaN material.

94. The semiconductor device of claim 12, comprising: